Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A memory device having plural DRAM sub-arrays, each with plural array rows, comprising:

an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and

refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request, wherein logically adjacent rows are placed in different sub-arrays,

wherein a first row is in a first sub-array and a second row is in a second sub-array, the second row being one logical row from the first row, and a third row is in the first sub-array and a fourth row is in the second sub-array, the fourth row being one logical row from the third row.

2. (Original) The memory device as claimed in claim 1, wherein the memory access request comprises a read access request.

3. (Original) The memory device as claimed in claim 2, further comprising a non-array row, external to the DRAM sub-arrays, for receiving from the DRAM sub-array referenced by the address of the read access request at least a portion of an array row corresponding to the address of the read access request.

4. (Cancel)

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~~5.~~ (Original) The memory device as claimed in claim 3, further comprising:

a tag register for storing at least a portion of the address of a read access request that last stored information into the non-array row; and

a comparator for signaling that the read access request may be serviced from the non-array row rather than the array row corresponding to the address of the read access request.

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6. (Original) The memory device as claimed in claim 1, wherein the memory access request comprises a write access request.

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7. (Original) The memory device as claimed in claim 6, further comprising a non-array row, external to the DRAM sub-arrays, for storing, prior to writing to the DRAM sub-array referenced by the address of the write access request, at least a portion of an array row corresponding to the address of the write request.

8. - 9. (Cancel)

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10. (Original) The memory device as claimed in claim 1, wherein the refresh circuitry comprises a refresh counter for storing a next array row to be refreshed in at least one of the plural DRAM sub-arrays.

11. (Previously Presented) A method of refreshing a memory device having a plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) placing logically adjacent rows in different sub-arrays, wherein a first row is in a first sub-array and a second row is in a second sub-array, the second row being one logical row from the first row, and a third row is in the first sub-array and a fourth row is in the second sub-array, the fourth row being one logical row from the third row;

(b) decoding an address of a memory request;

(c) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;

(d) refreshing, in response to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request; and

(e) executing the memory address request,

wherein steps (d) and (e) are performed contemporaneously.

12. (Original) The method as claimed in claim 11, wherein the memory access request comprises a read access request.

13. (Original) The method as claimed in claim 11, further comprising:

receiving, into a non array row external to the plural DRAM sub-arrays and from the DRAM sub-array referenced by the address of the read access request, at least a portion of an array row corresponding to the address of the read request.

14. - 15. (Cancel)

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~~16.~~ (Original) The method as claimed in claim 11, wherein the memory access request comprises a write access request.

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~~17.~~ (Original) The method as claimed in claim 14 ~~16~~, further comprising storing into a non-array row, external to the DRAM sub-arrays, prior to writing to the DRAM sub-array referenced by the address of the write access request, at least a portion of an array row corresponding to the address of the write request.

18. - 19. (Cancel)

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~~20.~~ (Original) The method as claimed in claim 11, further comprising updating a refresh counter to store a next array row to be refreshed in at least one of the plural DRAM sub-arrays.

21. - 24. (Cancel)

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~~25.~~ (Previously Presented) The memory device as claimed in claim 1, wherein every other logically adjacent row resides on a separate sub-array.

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~~26.~~ (Previously Presented) The memory device as claimed in claim 1, wherein even numbered rows and odd numbered rows reside on separate sub-arrays.

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27. (Previously Presented) A memory device having plural DRAM sub-arrays, each with plural array rows, comprising:

an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and

refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request, wherein logically adjacent rows are placed in different sub-arrays,

wherein each row of a first sub-array is L rows higher in logical memory than each corresponding row of a second sub-array, wherein L is an integer less than the maximum number of rows in a sub-array.

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28. (Previously Presented) A memory device having plural DRAM sub-arrays, each with plural array rows, comprising:

an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and

refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request, wherein logically adjacent rows are placed in different sub-arrays, and the logically adjacent rows in different sub-arrays comprise rows other than the last and first rows of consecutive sub-arrays.

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29. (Previously Presented) A memory device having plural DRAM sub-arrays, each with plural array rows, comprising:

an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and

refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request, wherein logically adjacent rows are placed in different sub-arrays;

wherein a first row is in physical memory row N of a first sub-array and a second row is in physical memory row M of a second sub-array, wherein the second row is absolutely higher in logical memory than the first row and the second row is X+(M-N) logical rows from the first row, wherein N and M are integers from 1 to K and X is an integer greater than -K and less than K, wherein K is the maximum number of rows in a sub-array.

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30. (Previously Presented) A method of refreshing a memory device having a plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) placing logically adjacent rows in different sub-arrays, and the logically adjacent rows in different sub-arrays comprise rows other than the last and first rows of consecutive sub-arrays;

(b) decoding an address of a memory request;

(c) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;

(d) refreshing, in response to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request; and

(e) executing the memory address request,

wherein steps (d) and (e) are performed contemporaneously.

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31. (Previously Presented) A method of refreshing a memory device having a plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) placing logically adjacent rows in different sub-arrays, wherein a first row is in physical memory row N of a first sub-array and a second row is in physical memory row M of a second sub-array, wherein the second row is absolutely higher in logical memory than the first row and the second row is X+(M-N) logical rows from the first row, wherein N and M are

integers from 1 to K and X is an integer greater than -K and less than K, wherein K is the maximum number of rows in a sub-array;

(b) decoding an address of a memory request;

(c) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;

(d) refreshing, in response to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request; and

(e) executing the memory address request,

wherein steps (d) and (e) are performed contemporaneously.